- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Specified From –40°C to 85°C and –40°C to 125°C
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
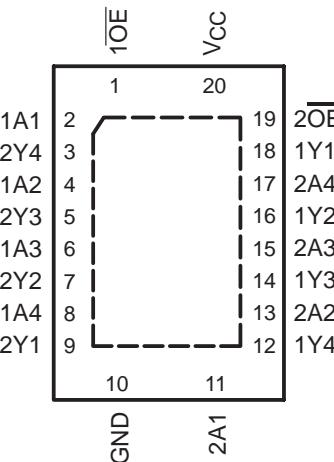
description/ordering information

This octal buffer/line driver is operational at 1.5-V to 3.6-V V_{CC}, but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		20	V_{CC}
1A1	2		19	2$\overline{OE}$
2Y4	3		18	1Y1
1A2	4		17	2A4
2Y3	5		16	1Y2
1A3	6		15	2A3
2Y2	7		14	1Y3
1A4	8		13	2A2
2Y1	9		12	1Y4
GND	10		11	2A1

RGY PACKAGE
(TOP VIEW)

	1$\overline{OE}$ (1)	V_{CC} (20)		
1A1	2		19	2$\overline{OE}$
2Y4	3		18	1Y1
1A2	4		17	2A4
2Y3	5		16	1Y2
1A3	6		15	2A3
2Y2	7		14	1Y3
1A4	8		13	2A2
2Y1	9		12	1Y4
	GND (10)	2A1 (11)		

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC244ARGYR	LC244A
	VFBGA – GQN	Reel of 1000	SN74LVC244AGQNR	LC244A
	VFBGA – ZQN (Pb-Free)		SN74LVC244AZQNR	
–40°C to 125°C	PDIP – N	Tube of 20	SN74LVC244AN	SN74LVC244AN
	SOIC – DW	Tube of 25	SN74LVC244ADW	LVC244A
		Reel of 2000	SN74LVC244ADWR	
	SOP – NS	Reel of 2000	SN74LVC244ANSR	LVC244A
	SSOP – DB	Reel of 2000	SN74LVC244ADBR	LC244A
	TSSOP – PW	Tube of 70	SN74LVC244APW	LC244A
		Reel of 2000	SN74LVC244APWR	
		Reel of 250	SN74LVC244APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC244ADGVR	LC244A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN74LVC244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS414W – NOVEMBER 1992 – REVISED MAY 2004

description/ordering information (continued)
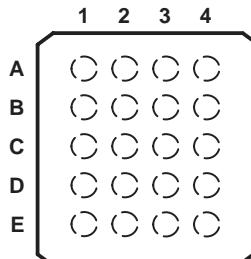
The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQN OR ZQN PACKAGE
(TOP VIEW)
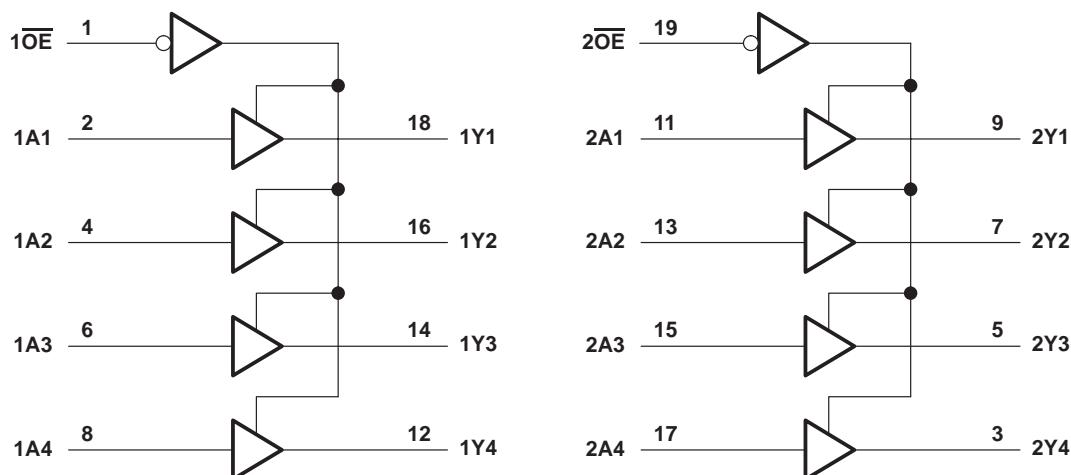
terminal assignments

	1	2	3	4
A	1A1	1$\overline{OE}$	V_{CC}	2$\overline{OE}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)

Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) .... –0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
    (see Note 1) .... –0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
    (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA

Continuous output current, I_O .... ±50 mA

Continuous current through V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W
                                     (see Note 3): DGV package .... 92°C/W
                                     (see Note 3): DW package .... 58°C/W
                                     (see Note 3): GQN/ZQN package .... 78°C/W
                                     (see Note 3): N package .... 69°C/W
                                     (see Note 3): NS package .... 60°C/W
                                     (see Note 3): PW package .... 83°C/W
                                     (see Note 4): RGY package .... 37°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

Power dissipation, P_{tot} (T_A = –40°C to 125°C) (see Notes 5 and 6) .... 500 mW

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
        2. The value of V_{CC} is provided in the recommended operating conditions table.
        3. The package thermal impedance is calculated in accordance with JESD 51-7.
        4. The package thermal impedance is calculated in accordance with JESD 51-5.
        5. For the DW package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
        6. For the DB, DGV, N, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

recommended operating conditions (see Note 7)

			$T_A = 25°C$		−40 TO 85°C		−40 TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4		−4		−4	mA
		V_{CC} = 2.3 V		−8		−8		−8	
		V_{CC} = 2.7 V		−12		−12		−12	
		V_{CC} = 3 V		−24		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	

NOTE 7: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			−40 TO 85°C		−40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −100 µA		1.65 V to 3.6 V	V_{CC}–0.2			V_{CC}–0.2		V_{CC}–0.3		V
	I_{OH} = −4 mA		1.65 V	1.29			1.2		1.05		
	I_{OH} = −8 mA		2.3 V	1.9			1.7		1.55		
	I_{OH} = −12 mA		2.7 V	2.2			2.2		2.05		
			3 V	2.4			2.4		2.25		
	I_{OH} = −24 mA		3 V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 µA		1.65 V to 3.6 V			0.1		0.2		0.3	V
	I_{OL} = 4 mA		1.65 V			0.24		0.45		0.6	
	I_{OL} = 8 mA		2.3 V			0.3		0.7		0.75	
	I_{OL} = 12 mA		2.7 V			0.4		0.4		0.6	
	I_{OL} = 24 mA		3 V			0.55		0.55		0.8	
I_I	V_I = 5.5 V or GND		3.6 V			±1		±5		±20	µA
I_{off}	V_I or V_O = 5.5 V		0			±1		±10		±20	µA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±1		±10		±20	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			1		10		40	µA
	3.6 V ≤ V_I ≤ 5.5 V†					1		10		40	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		5000	µA
C_i	V_I = V_{CC} or GND		3.3 V		4						pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5						pF

† This applies in the disabled state only.
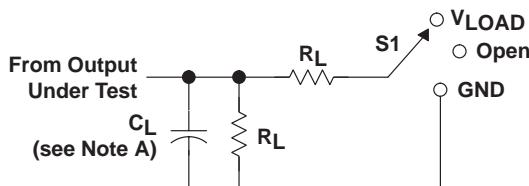
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			−40 TO 85°C		−40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5 V	1	7	14.4	1	14.9	1	16.4	ns
			1.8 V ± 0.15 V	1	5.9	10.4	1	10.9	1	12.4	
			2.5 V ± 0.2 V	1	4.2	7.4	1	7.9	1	10	
			2.7 V	1	4.2	6.7	1	6.9	1	8.2	
			3.3 V ± 0.3 V	1.5	3.9	5.7	1.5	5.9	1.5	7.2	
t_{en}	$\overline{OE}$	Y	1.5 V	1	8.3	17.8	1	18.3	1	19.8	ns
			1.8 V ± 0.15 V	1	6.4	12.1	1	12.6	1	14.1	
			2.5 V ± 0.2 V	1	4.6	9.1	1	9.6	1	11.7	
			2.7 V	1	5	8.4	1	8.6	1	10.3	
			3.3 V ± 0.3 V	1.5	4.5	7.4	1.5	7.6	1.5	9.4	
t_{dis}	$\overline{OE}$	Y	1.5 V	1	7.2	15.6	1	16.1	1	17.6	ns
			1.8 V ± 0.15 V	1	5.8	11.6	1	12.1	1	13.6	
			2.5 V ± 0.2 V	1	3.7	7.3	1	7.8	1	9.9	
			2.7 V	1	3.8	6.6	1	6.8	1	8.6	
			3.3 V ± 0.3 V	1.5	3.8	6.3	1.5	6.5	1.5	8	
$t_{sk(o)}$			3.3 V ± 0.3 V					1		1.5	ns

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	1.8 V	43	pF
			2.5 V	43	
			3.3 V	44	
	Outputs disabled	f = 10 MHz	1.8 V	1	
			2.5 V	1	
			3.3 V	2	

TEXAS
INSTRUMENTS
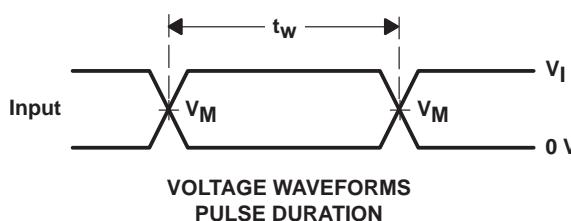
PARAMETER MEASUREMENT INFORMATION
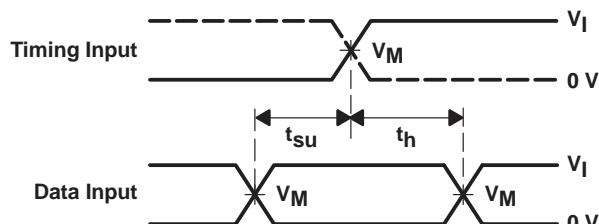
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
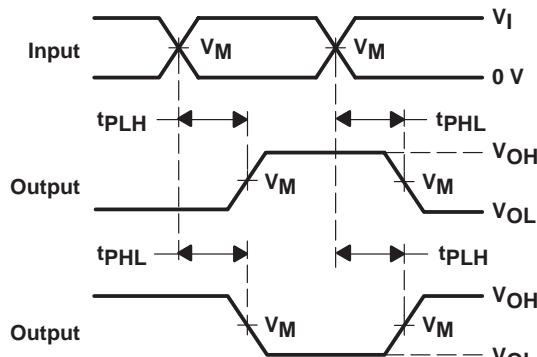
| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.5 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
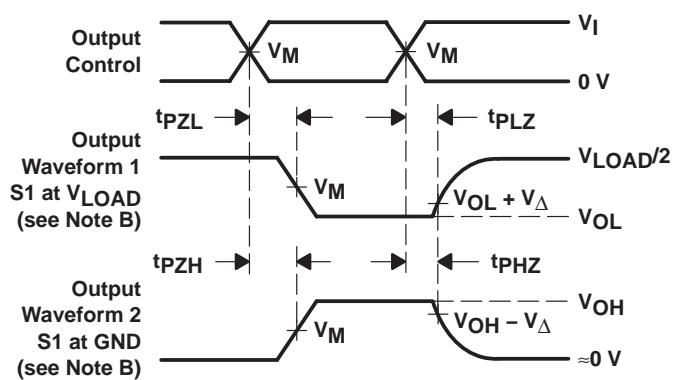
VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
**INVERTING AND NONINVERTING OUTPUTS**

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
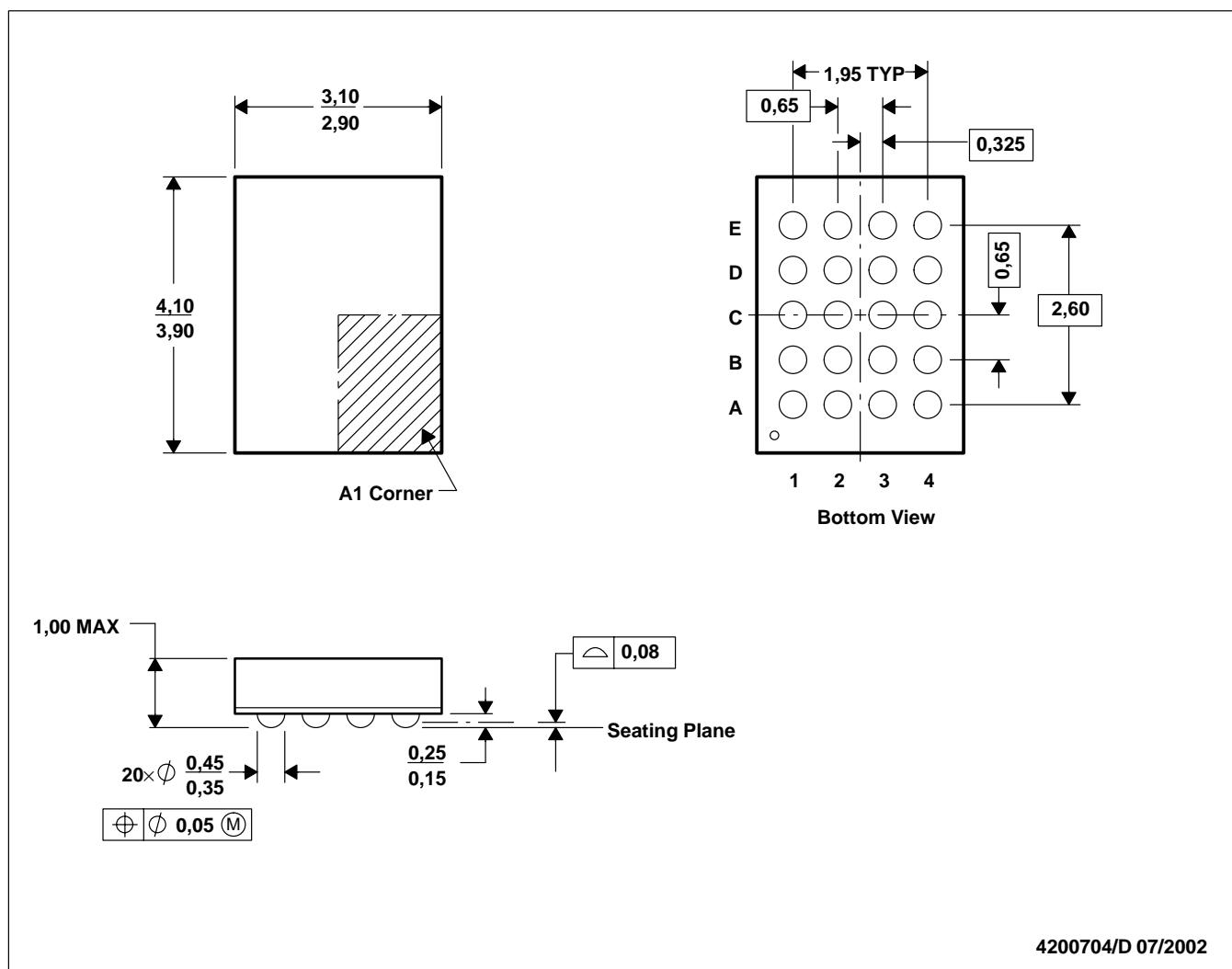
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

GQN (R-PBGA-N20)   **PLASTIC BALL GRID ARRAY**
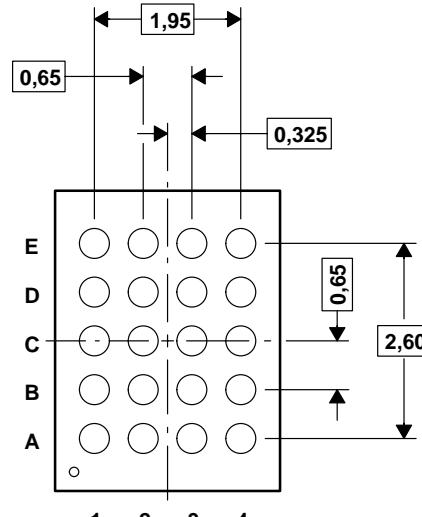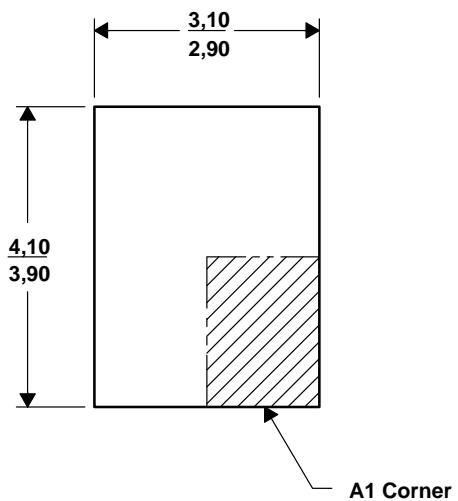
3,10
2,90

4,10
3,90

A1 Corner

1,95 TYP

0,65

0,325

E D C B A

0,65

2,60

1 2 3 4

Bottom View

1,00 MAX

0,08

Seating Plane

20×⌀ 0,45
0,35

0,25
0,15

⊕ ⌀ 0,05 Ⓜ

4200704/D 07/2002

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ configuration
D. Falls within JEDEC MO-225 variation BC.
E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.
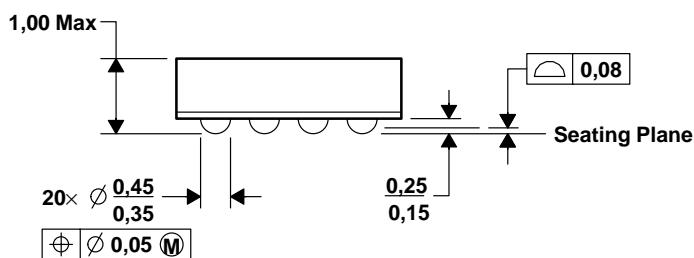
MicroStar Junior is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

ZQN (R-PBGA-N20)   **PLASTIC BALL GRID ARRAY**
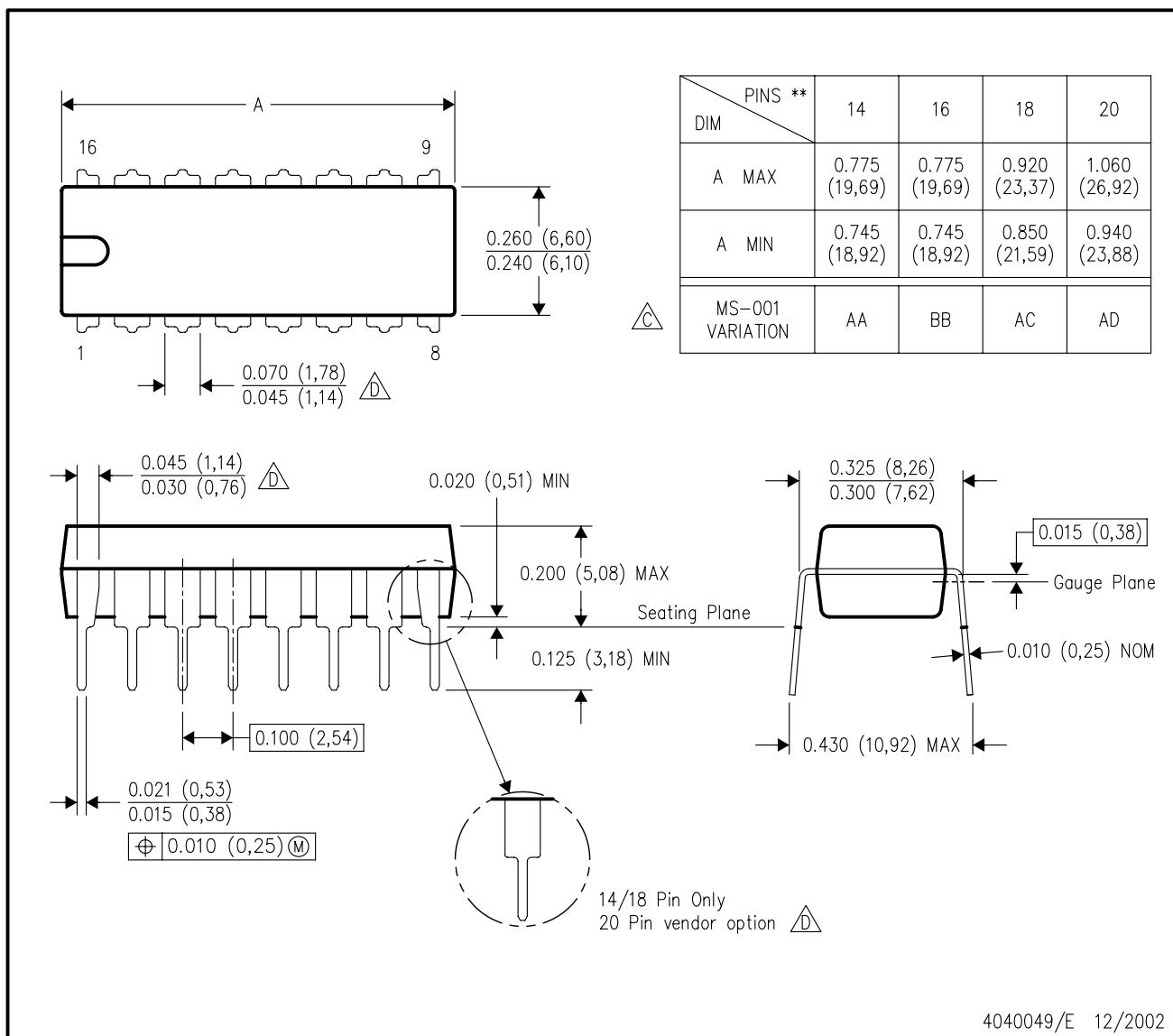
3,10
2,90

4,10
3,90

A1 Corner

1,95

0,65

0,325

E
D
C
B
A

1   2   3   4

0,65

2,60

Bottom View

1,00 Max

0,08

Seating Plane

20× ⌀ 0,45
        0,35

0,25
0,15

⊕ ⌀ 0,05 Ⓜ

4204492/A 06/2002

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. MicroStar Junior™ configuration.
        D. Fall within JEDEC MO-225 variation BC.
   E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead)SnPb).

MicroStar Junior is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265
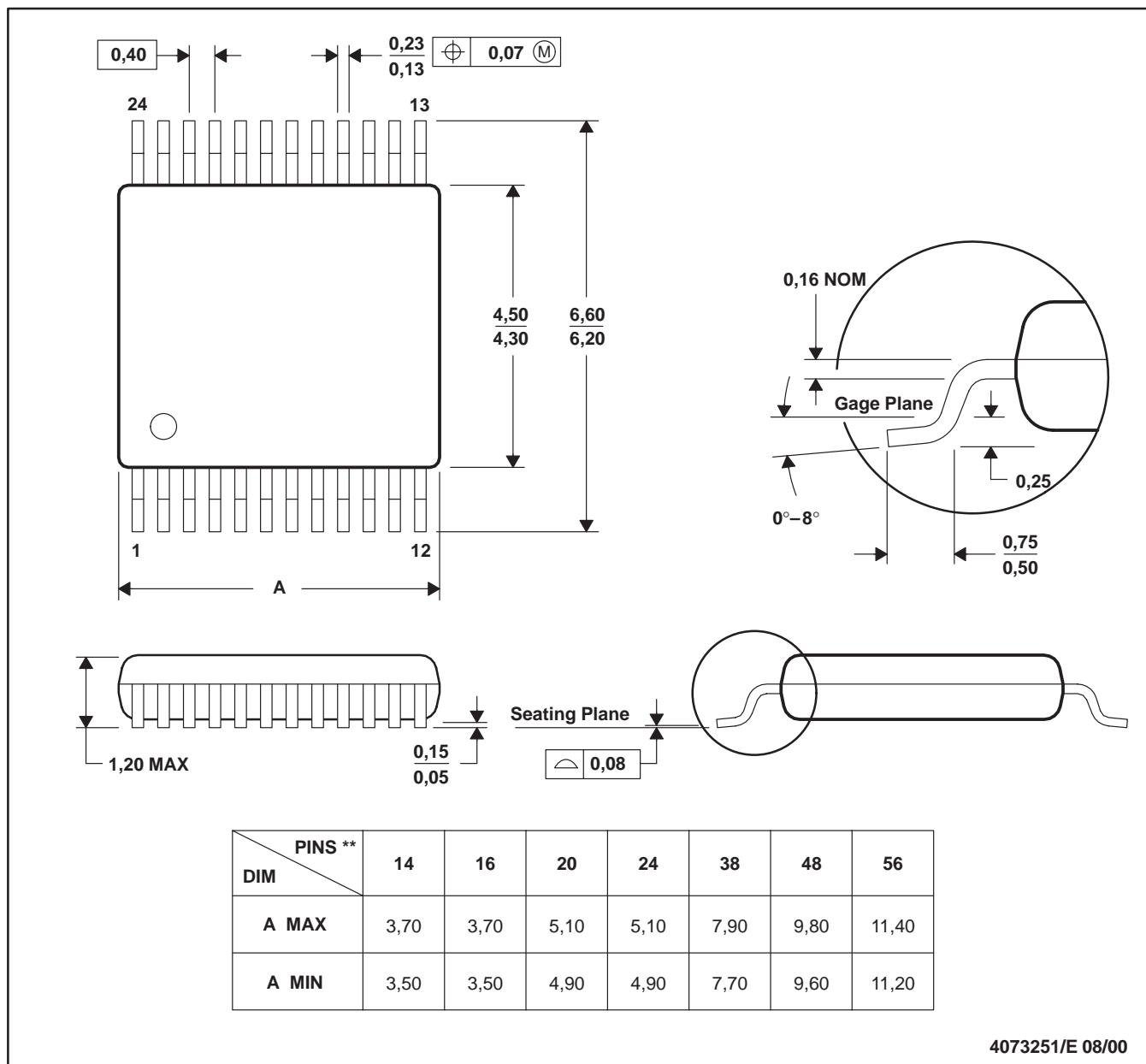
N (R−PDIP−T**)   **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

$\oplus$ 0.010 (0,25) ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
        C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
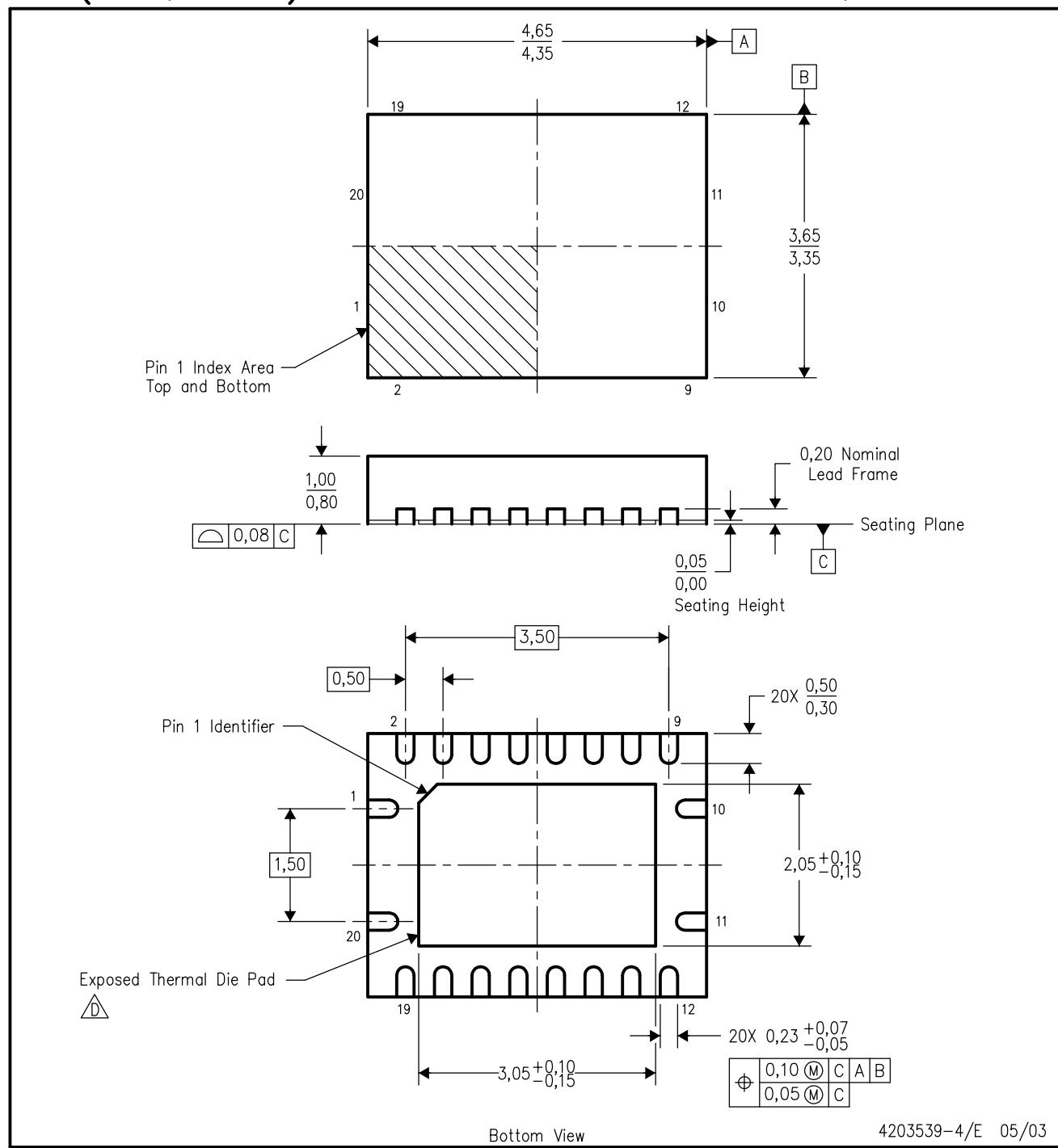
DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
                    14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

RGY (R−PQFP−N20)   **PLASTIC QUAD FLATPACK**

4,65 / 4,35 — A

B

19   12

20   11

3,65 / 3,35

1

Pin 1 Index Area
Top and Bottom

2   9

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,08 C

0,05 / 0,00
Seating Height

C

3,50

0,50

20X 0,50 / 0,30

Pin 1 Identifier

2   9

1   10

1,50

2,05 +0,10 / −0,15

20   11

Exposed Thermal Die Pad

D

19   12

3,05 +0,10 / −0,15

20X 0,23 +0,07 / −0,05

⊕ | 0,10 Ⓜ | C | A | B
   | 0,05 Ⓜ | C

Bottom View   4203539−4/E 05/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   QFN (Quad Flatpack No−Lead) package configuration.
          D.   The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
               This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
          E.   Package complies to JEDEC MO−241 variation BC.
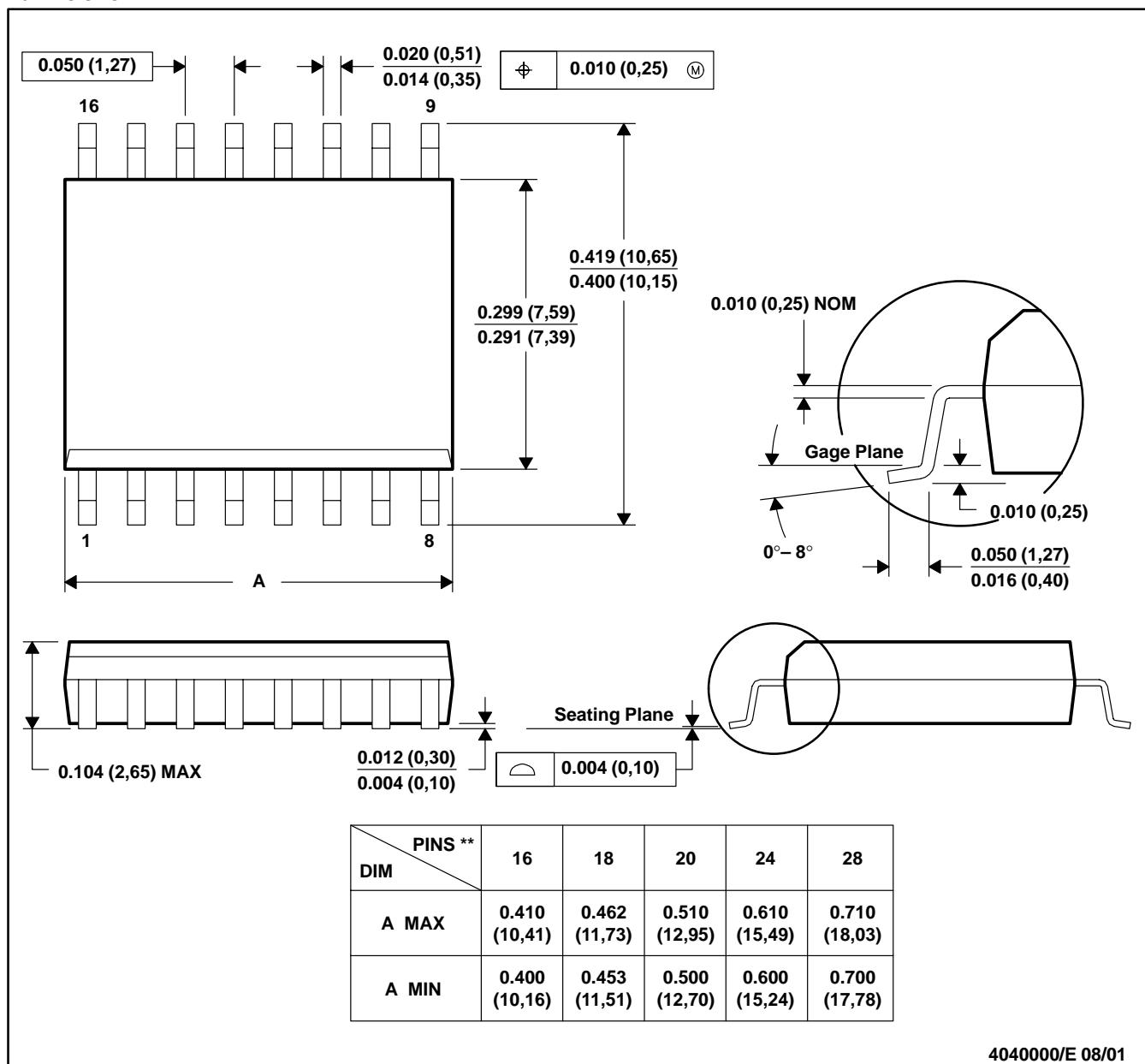
DW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN
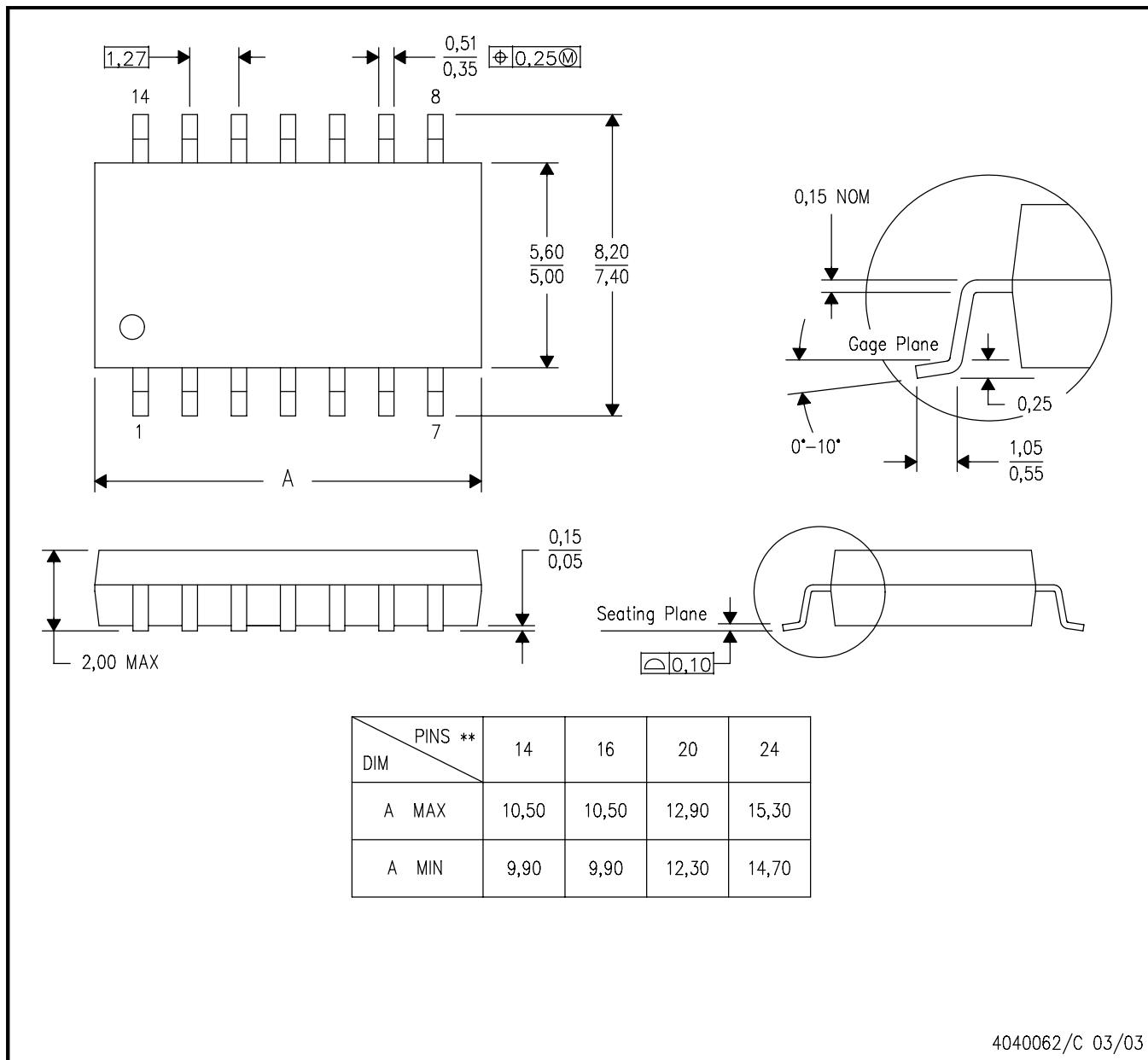
PINS ** DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA
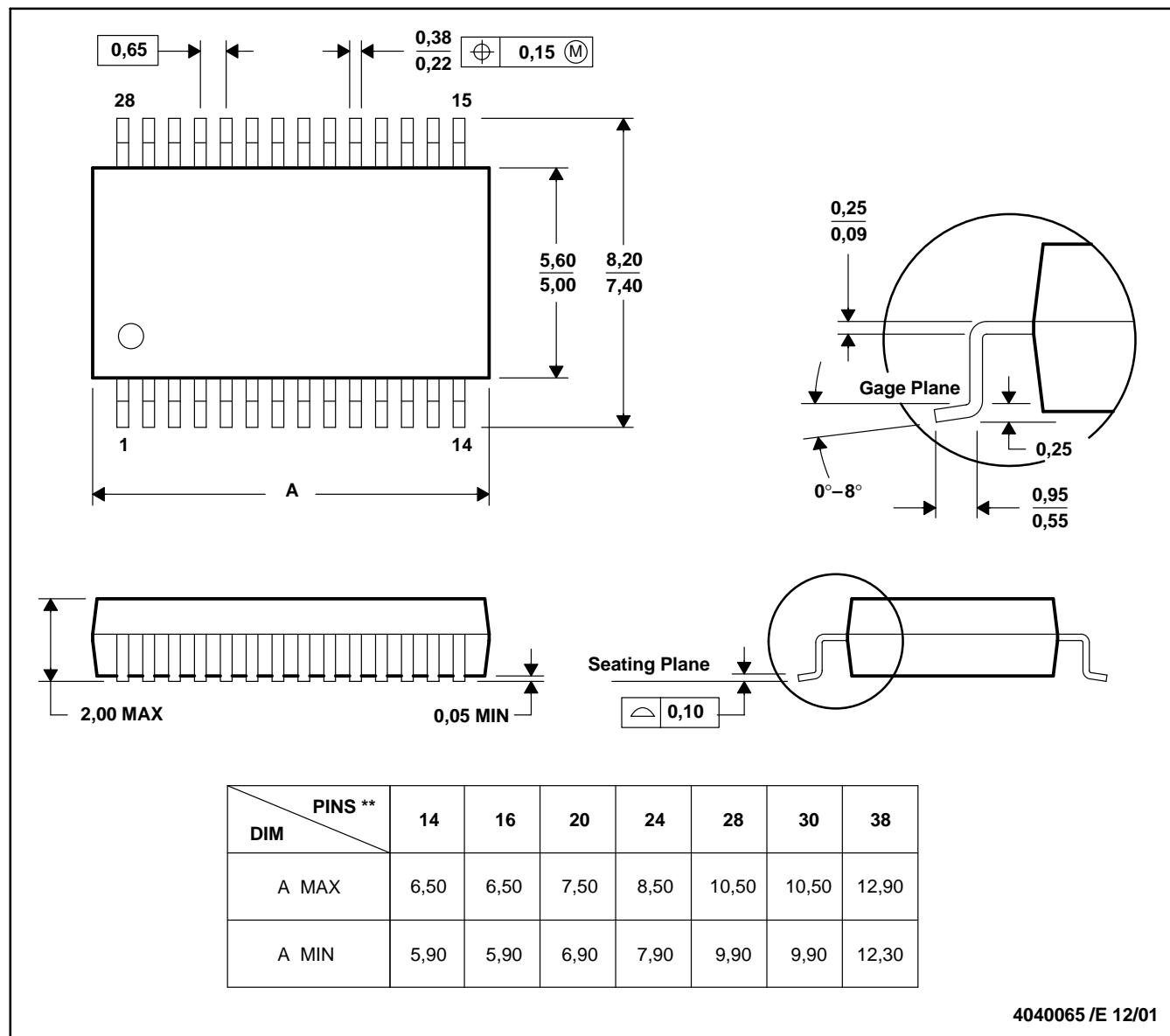
PLASTIC SMALL-OUTLINE PACKAGE

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
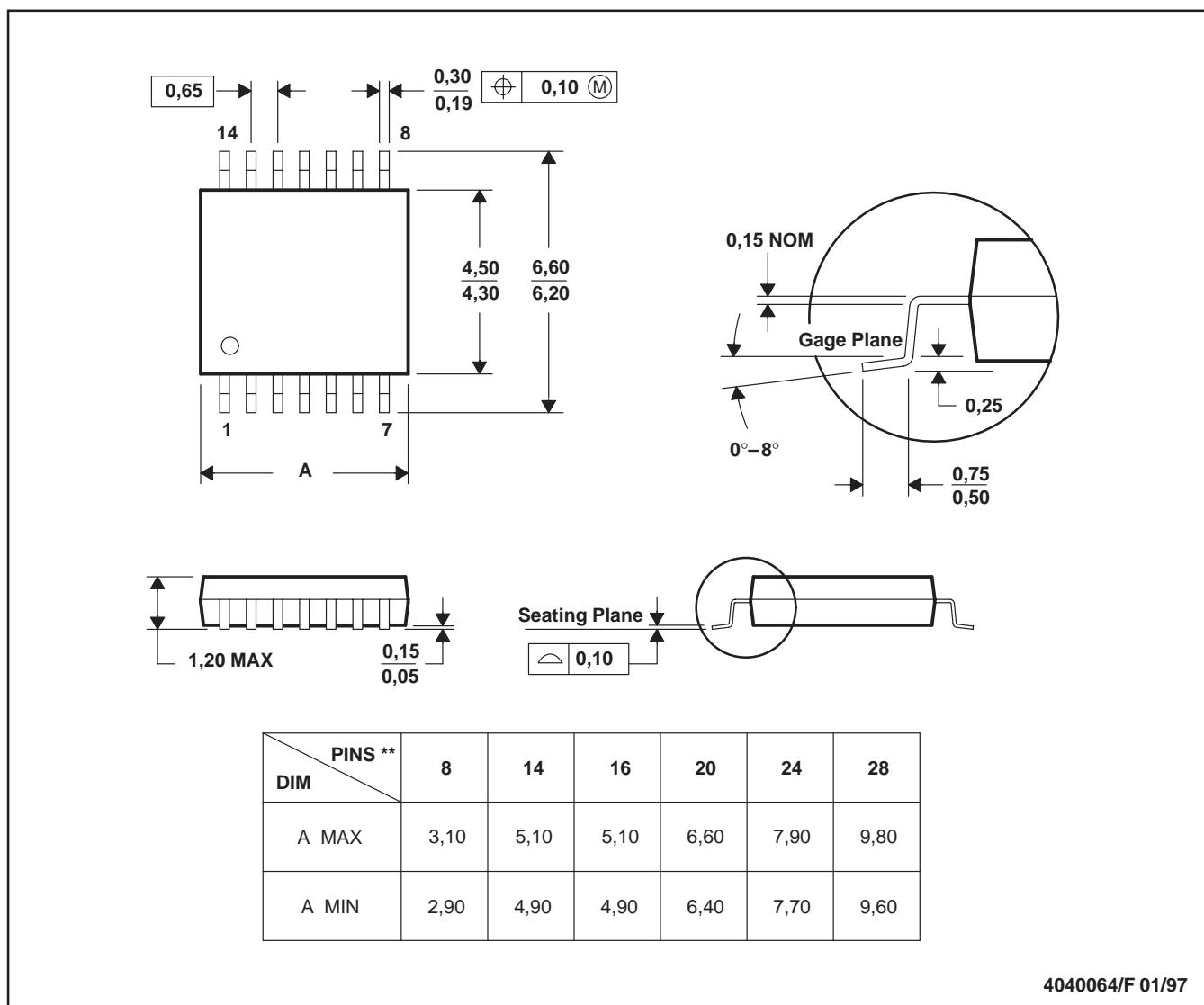
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
          D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                    Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated