

## Y-SUS Board SECTION (Overview)

Y-SUS Board develops the Y-Scan to the Y-Drive boards.

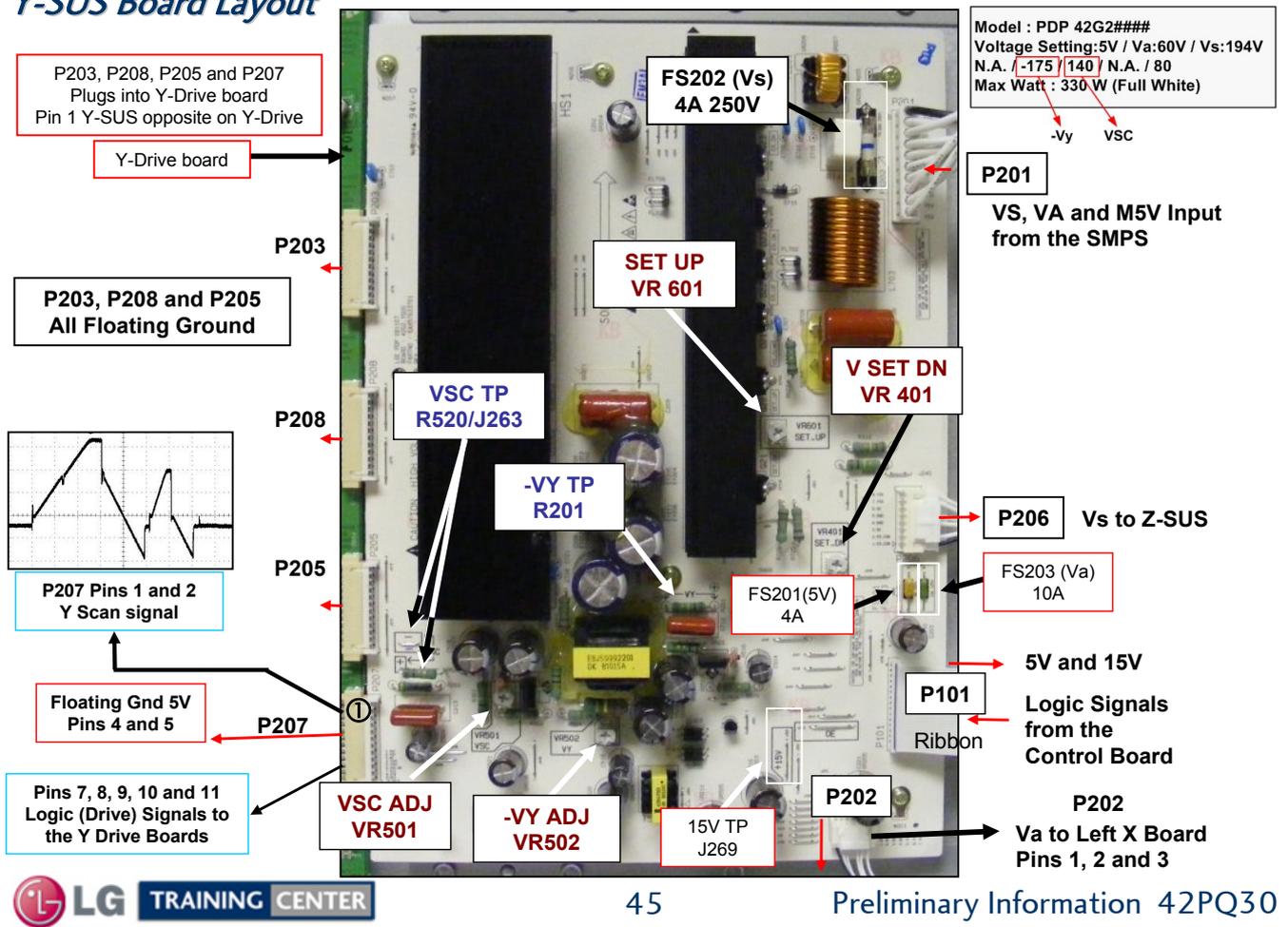
This Section of the Presentation will cover troubleshooting the Y-SUS Board for the Single Scan Plasma. Upon completion of the Section the technician will have a better understanding of the operation of the circuit and will be able to locate voltage and resistance test points needed for troubleshooting and alignments.

- Adjustments
- DC Voltage and Waveform Checks
- Resistance Measurements

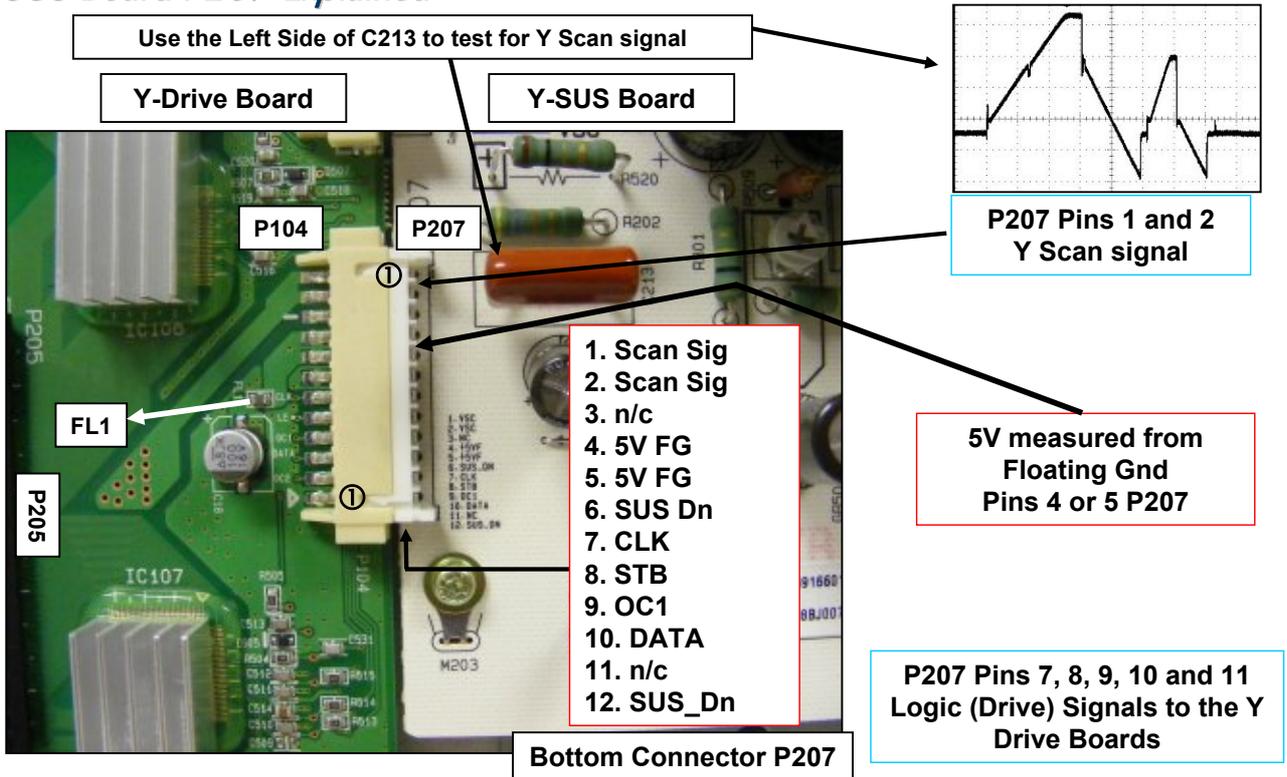
### Operating Voltages

<u>SMPS Supplied</u>	VA VS M5V	VA supplies the Panel Vertical Grid (Routed to the X-Boards) VS Supplies the Panel Horizontal Grid (Also routed to the Z-SUS) 5V Supplies Bias to Y-Z SUS, (Routed to the Control Board)
<u>Y-Z SUS Developed</u>	-VY VR502 VSC VR501 V SET UP VR601 V SET DN VR602 15V	-VY Sets the Negative excursion of the Y SUS Drive Waveform VSC Set the amplitude of the complex waveform. Ramp UP sets amplitude of the Top Ramp of the Drive Waveform V Set Down sets the Pitch of the Bottom Ramp of the Drive Waveform To the Control Board then routed to the Z-SUS board
<u>Floating Ground</u>	FG 5V	Used on the Y-Drive boards (Measured from Floating Gnd)

## Y-SUS Board Layout



## Y-SUS Board P207 Explained



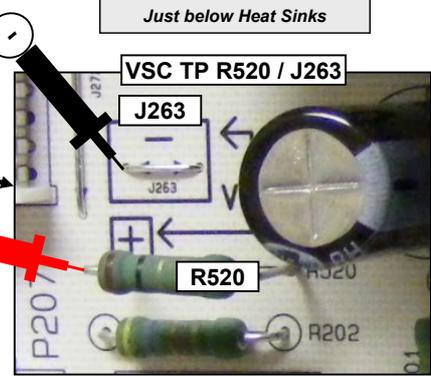
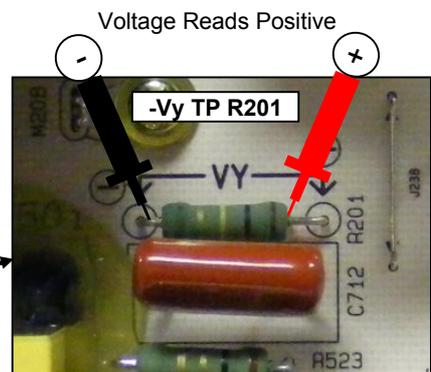
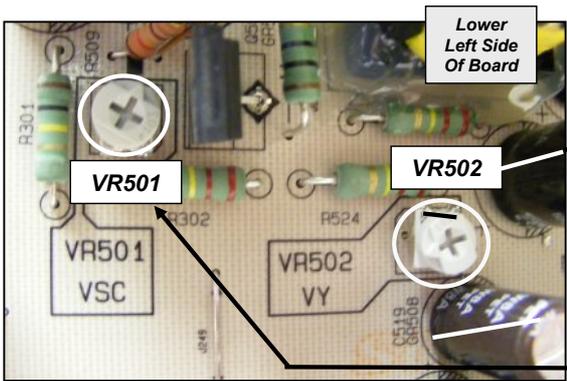
## VSC and -VY Adjustments

CAUTION: Use the actual panel label and not the book for exact voltage settings.

### Y SUSTAIN ADJUSTMENT DETAILS

**These are DC level  
Voltage Adjustments**

Model : PDP42G2####  
 809K442G2000568.AKLGDD  
 Voltage Setting: 5V / Va: 60 / Vs: 193  
 NA / -180 / 140 / N.A. / 80  
 -Vy VSC



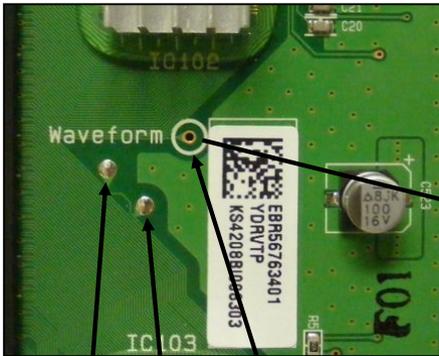
Set should run for 15 minutes, this is the "Heat Run" mode.  
 Set screen to "White Wash" mode or 100 IRE White input.

Adjust -Vy to Panel Label voltage (+/- 1V)  
 Adjust VSC to Panel Label voltage (+/- 1V)

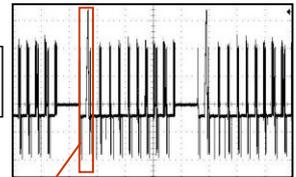


## Y-Drive Signal Overview

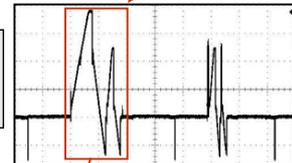
Y-Drive Board Test Point  
(Top of Y-Drive Board)



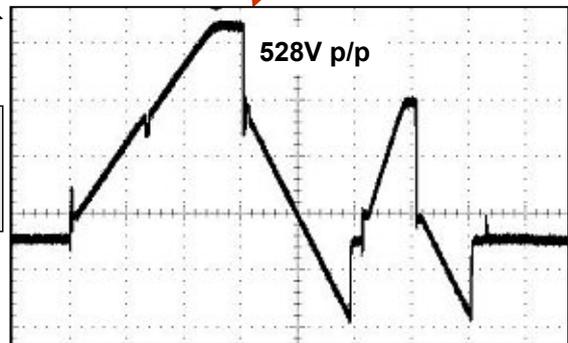
① Overall signal observed 4mS/div



② Highlighted signal from waveform above observed 400uS/div



**NOTE:** The Waveform Test Point is fragile. If by accident the land is torn and the run lifted, make sure there are no lines left to right in the screen picture.  
**NOTE:** The two test points just below and to the left will also work for the Y-Drive waveform Test Point.



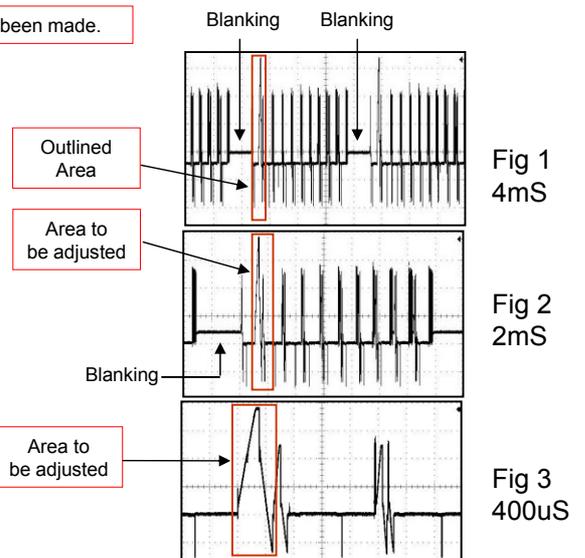
100uS

## Observing (Capturing) the Y-Drive Signal for Vsetup and Set Dn

Set must be in "WHITE WASH" All other DC Voltage adjustments should have already been made.

### Fig 1:

As an example of how to lock in to the Y-Drive Waveform. Fig 1 shows the signal locked in at 4ms per/div. Note the 2 blanking sections. The signal for SET-UP or SET-DN is outlined within the Waveform



### Fig 2:

At 2mSec per/division, the waveform area to use for SET-UP or SET-DN is now becoming clear.

### Fig 3:

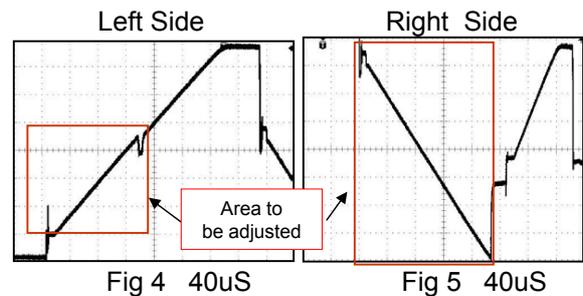
At 400us per/div. the signal for SET-UP or SET-DN is now easier to recognize. It is outlined within the Waveform

### Fig 4:

At 40uSec per/division, the adjustment for SET-UP can be made.

### Fig 5:

At 40uSec per/division, the adjustment for SET-DN can be made.



## V-Set Up and V-Set Down Adjustments

Y SUSTAIN ADJUSTMENT DETAILS (Vs, Va, VSC and -VY must have already been completed). Set in White Wash.

Observe the Picture while making these adjustments. Normally, they do not have to be done.

**Y-Drive Board Test Point**

**Waveform TP on the Y-Drive PWB**

VR601 Set-up  
160V ± 1V

VR401 Set-Dn  
185uSec ± 5uSec

50VAC rms    100V    100uS    483V p/p

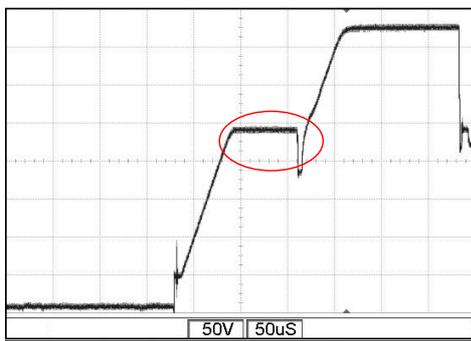
Connect Scope between Waveform TP on Y-Drive and Gnd

**SET-UP ADJUST:**  
1) Adjust **VR601** and set the **(A)** portion of the signal to match the waveform above.

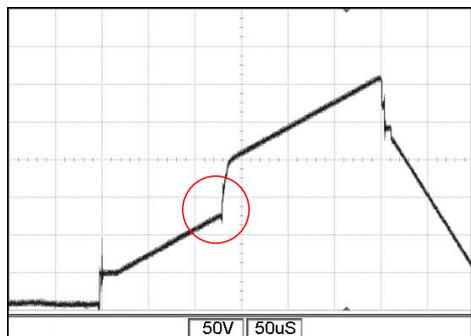
**SET-DN ADJUST:**  
2) Adjust **VR401** and set the **(B)** time of the signal to match the waveform above.

**ADJUSTMENT LOCATION:**  
Just to the bottom right of the right hand heat sink.

## V Set Up Too High or Low

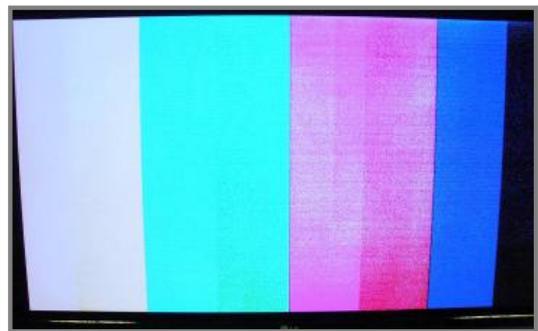


Ramp (Vset UP) too high

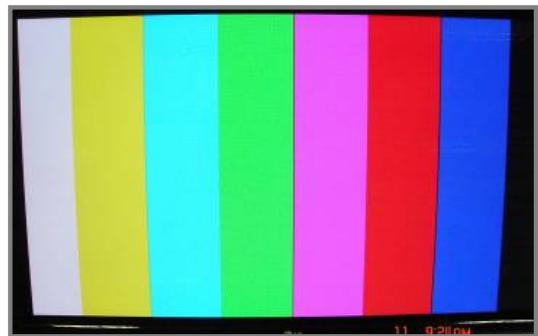


Ramp (Vset UP) too low

## Panel Waveform Adjustment



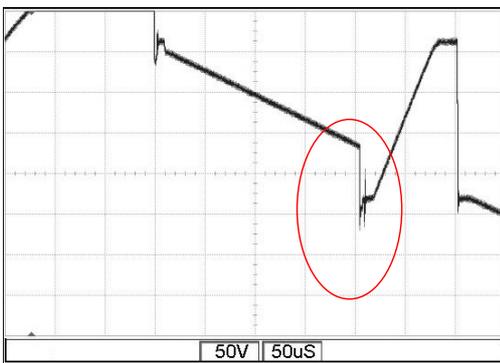
The center begins to wash out and arc due to **Vset UP** Peeking too late and alters the start of the **Vset DN** phase.



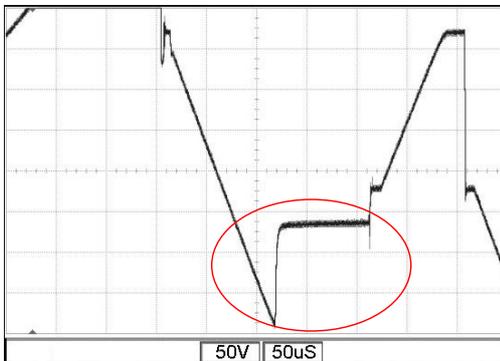
Very little alteration to the picture, the wave form indicates a distorted **Vset UP**. The peak widens due to the **Vset UP** peeking too quickly.

## V Set Dn Too High or Low

Vset Dn swing is Minimum 110uS Max 200uS+



Vset DN too high

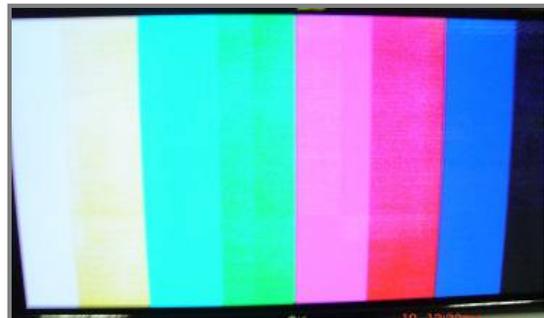


Vset DN too low

## Panel Waveform Adjustment

**NOTE: If VSET-DN is too high, this set will go to excessive bright, then shutdown. To correct, remove the LVDS from control Board and make necessary adjustments.**

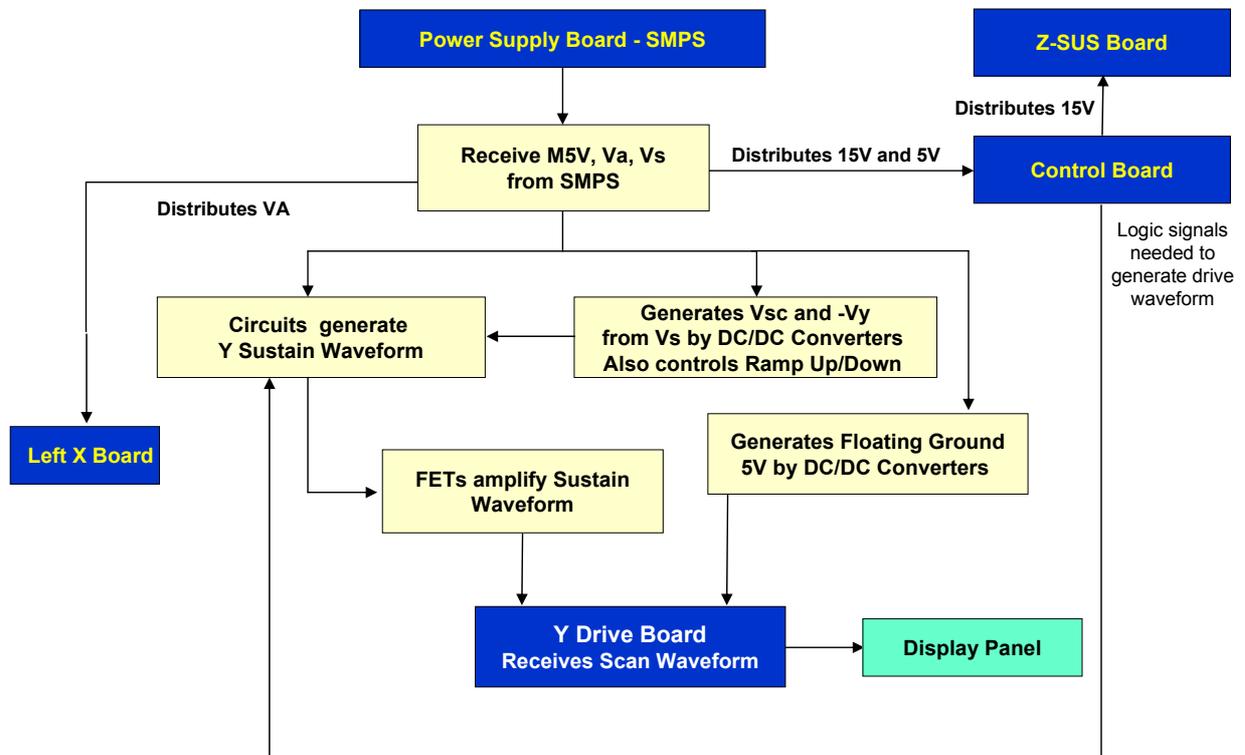
All of the center washes out due to increased Vset\_DN time.



The center begins to wash out and arc due to decreased Vset DN time.

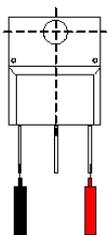
## Y SUS Block Diagram

Block Diagram of Y-Sustain Board



## Y-SUS How to Check the Output FETs

Name is printed on the components. Readings "In Circuit".

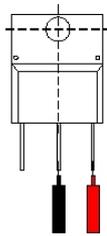


### IRFP4332

Forward: 0.5V ~ 0.7V  
Reverse: 1.1V

### IRGP4086

Forward: 0.6V ~ 0.7V  
Reverse: 1.3V

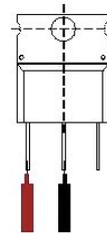


### IRFP4332

Forward: 0.4V ~ 0.5V  
Reverse: Open

### IRGP4086

Forward: 0.39V ~ 0.5V  
Reverse: Open



### IRFP4332

Forward: 1.6V  
Reverse: Open

### IRGP4086

Forward: 0.6V ~ 0.7V  
Reverse: 1.3V



### RF2001

Forward: Shorted  
Reverse: Shorted

### 30N45T

Forward: 0.6V  
Reverse: Shorted

### K3667

Forward: 0.22V  
Reverse: Open



### RF2001

Forward: 0.4V  
Reverse: Open

### 30N45T

Forward: 0.6V  
Reverse: Shorted

### K3667

Forward: 0.5V  
Reverse: Open



### RF2001

Forward: 0.38V  
Reverse: Open

### IRGP4086

Forward: 0.39V ~ 0.5V  
Reverse: Open

### K3667

Forward: 0.4V ~ 0.5V  
Reverse: Open

## *Y-SUS P201 to SMPS P812 Voltage and Diode Checks*

### Voltage and Diode Checks Measurement

**P201 Connector "Y-SUS" to "Power Supply Board" P811**

Pin	Label	STBY	Run	Diode Mode
1	Vs	0V	*193V	Open
2	Vs	0V	*193V	Open
3	NC	NC	NC	NC
4	Gnd	Gnd	Gnd	Gnd
5	Gnd	Gnd	Gnd	Gnd
6	Va	0V	*60V	Open
7	Va	0V	*60V	Open
8	Gnd	Gnd	Gnd	Gnd
9	M5V	0V	5V	1.1V
10	M5V	0V	5V	1.1V

**\* Note: This voltage will vary in accordance with Panel Label**

Diode Mode Readings taken with all Connectors Disconnected. DVM in Diode Mode.



## *Y-SUS P202 to X Drive P211 and P311 Voltage and Diode Checks*

### Voltage and Diode Mode Measurements for the Y SUS Board

#### P202 Connector "Y-SUS Board" to "X-Drive" Left P233

Pin	Label	STBY	Run	Diode Mode
1	Gnd	Gnd	Gnd	Gnd
2	Gnd	Gnd	Gnd	Gnd
3	Gnd	Gnd	Gnd	Gnd
4	nc	nc	nc	nc
5	VA	0V	*60V	Open
6	VA	0V	*60V	Open
7	VA	0V	*60V	Open

**\* Note: This voltage will vary in accordance with Panel Label**

Diode Mode Readings taken with all Connectors Disconnected. DVM in Diode Mode.



## *Y-SUS P801 to Z Drive P1 Voltage and Diode Checks*

### Voltage and Diode Mode Measurements for the Y SUS Board

**P206 Connector Y-SUS to Z Drive P1 Plug Information**

Pin	Label	STBY	Run	Diode Mode
1	Er Com	0V	* 94.9V	Open
2	Er Com	0V	*94.9V	Open
3	nc	nc	nc	nc
4	Gnd	Gnd	Gnd	Gnd
5	Gnd	Gnd	Gnd	Gnd
6	nc	nc	nc	nc
7	VS	0V	*193V	Open
8	VS	0V	*193V	Gnd

**\* Note: This voltage will vary in accordance with Panel Label**

Diode Mode Readings taken with all Connectors Disconnected. DVM in Diode Mode.



## P101 Y-SUS to Control Board P111 Plug Information

### Voltage Measurements for the Y SUS Board

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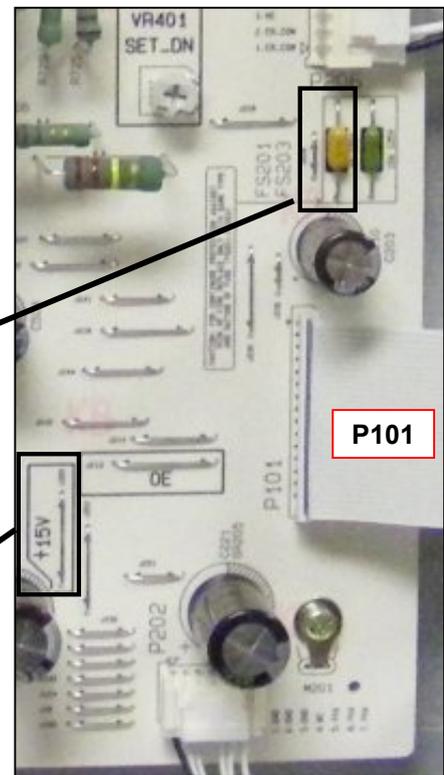
These Connector pins are too close to read without possible damage to the Board

Actually a 30 Pin Connector "Measurements can be made on the Control Board

Y-SUS Board B+ checks for the P101 Connector.

**FS201**  
**5V to run the Control Board.**  
Also sent to the Z-SUS Board.  
Routed through the Control Board.  
Leaves the Control Board on P101 pins 10.  
Standby: 0V    Run: 5V    Diode Check: 1.1V

**15V Test Point**  
**17V to run the Z-SUS Board.**  
Routed out P101 through the Control Board.  
Leaves the Control Board on P101 pins 11 and 12.  
Standby: 0V    Run: 15V    Diode Check: 0.78V



## Y-SUS P101 to Control P111 Voltage and Diode Checks

“Y-SUS” P101 Connector to “Control Board” P111

Pin	Label	STBY	Run	Diode Mode
1	Gnd	Gnd	0V	Gnd
3	n/a	0V	0.1V	0.65V
5	n/a	0V	1.28V	0.65V
7	n/a	0V	0V	0.65V
9	n/a	0V	0.6V	0.65V
11	n/a	0V	2.96V	0.65V
13	n/a	0V	1.4V	0.65V
15	n/a	0V	0V	0.65V
17	n/a	0V	1.89V	0.65V
19	n/a	0V	2.16V	0.65V
21	Gnd	Gnd	Gnd	Gnd
23	Gnd	Gnd	Gnd	Gnd
25	5V	0V	5V	0.44V
27	5V	0V	5V	0.44V
29	15V	0V	15V	Open

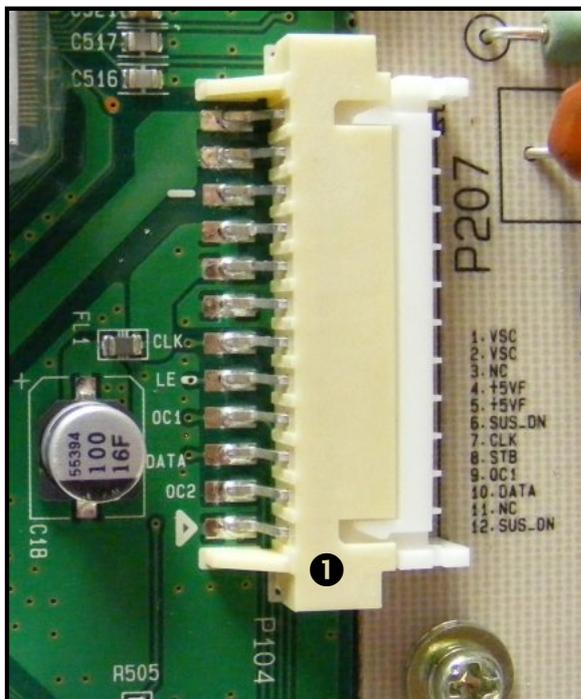
Pin	Label	STBY	Run	Diode Mode
2	n/a	0V	0.12V	0.65V
4	n/a	0V	0.13V	0.65V
6	n/a	0V	0.2V	0.65V
8	n/a	0V	1.05V	0.65V
10	n/a	0V	0.17V	0.65V
12	n/a	0V	2.5V	0.65V
14	n/a	0V	0V	0.65V
16	n/a	0V	0V	0.65V
18	n/a	0V	0V	Open
20	Gnd	Gnd	Gnd	Gnd
22	Gnd	Gnd	Gnd	Gnd
24	5V	0V	5V	0.44V
26	5V	0V	5V	0.44V
28	5V	0V	5V	0.44V
30	15V	0V	15V	Open

Diode Mode Readings taken with all Connectors Disconnected. DVM in Diode Mode.

## Y-SUS P207 Voltage Readings

All voltages taken from Floating Ground.

*Warning: Do not hook scope ground up unless set plugged into an isolation transformer.*

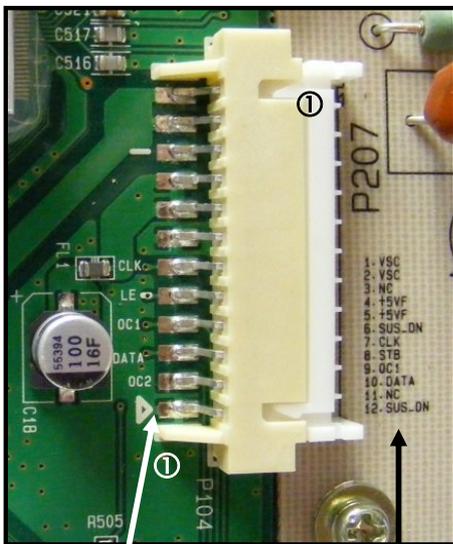


P207		
Pin	Label	Voltage
1)	VSC	140V
2)	VSC	140V
3)	Nc	
4)	5V VF	5V
5)	5V VF	5V
6)	SUS_DN	FGnd
7)	CLK	0.96V
8)	STB	2.3V
9)	OC1	2.3V
10)	DATA	0V
11)	Nc	
12)	SUS_DN	FGnd

## Y-SUS P207 (Drive Output Plug) TESTING

P104 OF THE Y-DRIVE Board      P207 OF THE Y-DRIVE Board

**CHECKING THE Y-SUS Board  
Disconnected from the Y-DRIVE Board**



Pin 1  
Floating  
Ground

Pin 1 on Y-SUS  
is backwards  
compared to  
Y-Drive

**Readings from Floating Ground (Pin 1)**

		RED LEAD Blk Lead FG	BLACK LEAD Red Lead FG
Y Drive Sig	1.) VSC	Open	Open
Y Drive Sig	2.) VSC	Open	Open
	3.) nc	Open	Open
	4.) FG+5V	1.78V	0.52V
	5.) FG+5V	1.78V	0.52V
Floating Gnd	6.) SUS Dn	0V	0V
	7.) CLK	1.57V	0.59V
	8.) LE	1.57V	0.59V
	9.) OC1	1.67V	0.63V
	10.) Data	1.57V	0.59V
	11.) nc	1.67V	0.65V
Floating Gnd	12.) SUS Dn	0V	0V

Meter in the Diode Mode

## Y-SUS FG5V, FG15V And 17V Testing

